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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/017,114	10/24/2001	Etsuko Fujimoto	SEL 283	4545

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EXAMINER	
DANG, PHUC T	

ART UNIT	PAPER NUMBER
2818	

DATE MAILED: 07/02/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/017,114	FUJIMOTO ET AL.	
	Examiner	Art Unit	
	PHUC T DANG	2818	

-- Th MAILING DATE of this communication appears on the cover she t with the correspond nc address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *amendment filed on May 24, 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-21 and 24-50* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-19,21-36,38-48 and 50* is/are rejected.

7)☒ Claim(s) *20,37 and 49* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *24 October 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. §§ 119 and 120

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

13)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application) since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

a) ☐ The translation of the foreign language provisional application has been received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121 since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Response to Arguments

1. Applicant's arguments filed on May 24, 2004 with respect to claims 1-21 and 24-50 have been considered but are moot in view of the new ground(s) of rejection.

Oath/Declaration

2. The oath/declaration filed on October 24, 2001 is acceptable.

Priority

3. Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

Specification

4. The specification has been checked to the extent necessary to determine the presence of all possible minor errors. However, the applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 1-9, 11-19, 21, 24-26, 28-36, 38, 40-48 and 50 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sakama et al. (U.S. Patent No. 6,632,708 B2) in view of Zamazaki (U.S. Patent No. 6,118,148).

Regarding claims 1 and 3-4, Sakama discloses a semiconductor device including thin film transistor comprising:

a semiconductor film (103, 104, 105, Fig. 6A) on an insulating surface;

an insulating film (106, Fig. 6A) over the semiconductor film;

a gate electrode (117, Fig. 6C) over the insulating film; where the semiconductor film including:

a channel forming region (Fig. 7A) overlapped with the gate electrode (124, Fig. 7A);

an impurity region (Fig. 7A) in contact with the channel forming region (Fig. 7A).

Regarding claims 2, 24-25, Sakama discloses all the features of the claim 1 as discussed above including an offset region (Fig. 7C) in contact with the channel forming region and an impurity region in contact with the offset region (Fig. 7C).

Sakama discloses all the limitations of the claimed invention as discussed above, but does not disclose the impurity region has a concentration distribution in which an impurity concentration is continuously increased with distance from the channel forming region in a channel length direction.

Zamazaki, however, discloses the impurity region has a concentration distribution in which an impurity concentration is continuously increased with distance from the channel forming region in a channel length direction [col. 20, lines 59-col. 21, lines 6].

It would have been obvious to one having ordinary skilled in the art at the time the invention was made to apply the teaching of Zamazaki to Sakama as discusses above such that the impurity region has a concentration distribution in which an impurity

concentration is increased with distance from the channel forming region for a purpose of improving the thin film transistor of a semiconductor device.

Regarding claims 5 and 26, Sakama discloses the thin film transistor is a c-channel thin film transistor [Fig. 8].

Regarding claim 6, Sakama discloses a semiconductor device comprising:

an pixel portion and a driving circuit on an insulating surface [Fig. 8];

an n-channel thin film transistor and a p-channel thin film transistor in the driving circuit [Fig. 8];

a pixel thin film transistor including a semiconductor film in the pixel portion, the semiconductor film including a channel forming region and an impurity region [Fig. 9B];

a pixel electrode (607, Fig. 11) connected to the pixel thin film transistor (600, Fig. 11) in the pixel portion.

Sakama discloses all the limitations of the claimed invention as discussed above, but does not disclose the impurity region has a concentration distribution in which an impurity concentration is increased with distance from the channel forming region.

Zamazaki, however, discloses the impurity region has a concentration distribution in which an impurity concentration is increased with distance from the channel forming region [col. 20, lines 59-col. 21, lines 6].

Regarding claim 7, Suzawa discloses a gate electrode in the n-channel thin film transistor, the gate electrode having a taper portion; an impurity region in the n-channel thin film transistor, wherein the taper portion is overlapped with the impurity region with an insulating film interposed therebetween.

It would have been obvious to one having ordinary skilled in the art at the time the invention was made to apply the teaching of Suzawa to Sakama as discusses above such that the gate electrode in the n-channel thin film transistor, the gate electrode having a taper portion; an impurity region in the n-channel thin film transistor, wherein the taper portion is overlapped with the impurity region with an insulating film interposed for a purpose of improving the thin film transistor of a semiconductor device.

Regarding claim 8, Sakama discloses an offset region between the channel forming region and the impurity region in the pixel thin film transistor [Fig. 8].

Regarding claim 9, Sakama discloses a gate electrode in the pixel thin film transistor, wherein the gate electrode is not overlapped with the channel forming region with an insulating film interposes in the pixel thin film transistor [Fig. 8 and col. 15, lines 64-col. 16, lines 2].

Regarding claims 11, 28 and 40, Sakama discloses the impurity region includes one of a source region and a drain region [Fig. 7A].

Regarding claims 12-14, 29-31 and 41-43, Sakama discloses some types of the concentration distribution of the impurity region [col. 4, lines 60-67].

Regarding claims 15, 32 and 44, Zamazaki discloses the impurity concentration is a concentration of an impurity to impart a one conductivity type to the semiconductor film [col. 1, lines 48+].

It would have been obvious to one having ordinary skilled in the art at the time the invention was made to apply the teaching of Zamazaki to Sakama as discusses above such that the impurity concentration is a concentration of an impurity to impart an one

conductivity type to the semiconductor film for a purpose of improving the thin film transistor of a semiconductor device.

Regarding claims 16-17, 33-34 and 45-46, Sakama discloses the semiconductor device is a liquid crystal and an El module [col. 1, lines 40+].

Regarding claims 18, 35 and 47, Sakama discloses the impurity is formed on both sides of the channel forming region [Fig. 7A].

Regarding claims 19, 36 and 48, Sakama discloses a thickness of the insulating film is different between a first region at a largest distance from the channel forming region and a second region at a smallest distance [Figs. 7A-7C].

Regarding claims 21, 38 and 50, Sakama discloses the semiconductor device is selected from the group consisting of a video camera, a digital camera, a projector, a goggle type display, a car navigation system, a personal computer and a portable information terminal [Figs. 16A-16F].

6. Claims 10, 27 and 39 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sakama et al. in view of Zamazaki and further in view of Hashimoto et al. (U.S. patent No. 6,587,165 B2).

Sakama and Zamazaki disclose all the features of the claimed invention as discussed above, but do not disclose the gate electrode includes a first conductive layer and a second conductive layer on the first conductive layer.

Hashimoto, however, disclose the gate electrode includes a first conductive layer and a second conductive layer on the first conductive layer [col. 10, lines 23-30].

It would have been obvious to one having ordinary skilled in the art at the time the invention was made to apply the teaching of Hashimoto et al. to Sakama and Zamazaki

discussed above such that the gate electrode includes a first conductive layer and a second conductive layer on the first conductive layer for a purpose of improving the thin film transistor of semiconductor device.

Allowable Subject Matter

7. Claims 20, 37 and 49 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claim.

Conclusion

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Phuc T. Dang whose telephone number is (571) 272-1776. The examiner can normally be reached on 8:00 am-5:00 pm.

9. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David C. Nelms can be reached on 703-308-4910. The fax phone numbers for the organization where this application or proceeding is assigned are 703-308-7722 for regular communications and 703-872-9306 for After Final communications.

10. Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

Phuc T. Dang PD

Primary Examiner

Art Unit 2818